

X-1270 US
10/792,153

PATENT
Conf. No.: 4867



IN THE UNITED STATES PATENT OFFICE

Applicant: Robert E. Eccles
Assignee: Xilinx, Inc.
Title: Method and Apparatus for Design Verification with
Equivalency Checking
Serial No.: 10/792,153 Filed: 03-02-2004
Examiner: Phallaka Kik Art Unit: 2825
Docket No.: X-1270 US Conf. No.: 4867

Mail Stop Amendment
COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450

AMENDMENT IN RESPONSE TO FIRST OFFICE ACTION

Dear Sir:

In response to the First Office Action mailed from the Patent Office on April 5, 2006, please replace/substitute the following claims as indicated.

Amendments to the Specification appear on page 2 of this paper.

Amendments to the Claims are reflected in the listing of claims which begins on page 3 of this paper.

Remarks/Arguments begin on page 11 of this paper.